



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/674,926

09/30/2003

Claus Michael Olsen

YOR920030005

5166

34663 7590 05/16/2008

MICHAEL J. BUCHENHORN  
8540 S.W. 83 STREET  
MIAMI, FL 33143

EXAMINER

BRADLEY, MATTHEW A

ART UNIT

PAPER NUMBER

2187

NOTIFICATION DATE

DELIVERY MODE

05/16/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

MICHAEL@BUCHENHORN.COM  
ANA@BUCHENHORN.COM

<b>Office Action Summary</b>	<b>Application No.</b> 10/674,926	<b>Applicant(s)</b> OLSEN ET AL.	
	<b>Examiner</b> MATTHEW BRADLEY	<b>Art Unit</b> 2187	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 January 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 21-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Response to Amendment*

This Office Action has been issued in response to amendment filed 11 January 2008. Applicant's arguments have been carefully and fully considered but they are not persuasive. Accordingly, this action has been made FINAL.

### *Claim Status*

Claims 21-40 remain pending and are ready for examination.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims **21-35** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Independent claim 21 recites, '...excluding storing only minimally used portions of information...' Referring back to Applicant's specification, at least insofar as it appears to be clear, there appears to be no support for excluding storing only minimally used portions of information.

Claims **21-35** and **40** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Independent claim 21 and independent claim 40 recite, 'always consumes [uses] more energy.' Referring back to Applicant's specification, at least insofar as it appears to be clear, there appears to be no support for the first level **always** consuming more energy than the second level.

Any claim not specifically addressed is rejected to at least by virtue of its dependency.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **21-26, 29-31, 33, and 37-38** are rejected under 35 U.S.C. 102(e) as being anticipated by Rudelic et al (U.S. 2004/0255283), hereinafter referred to as Rudelic.

As per independent claim **21**, Rudelic teach,

- first and second of levels of a non-volatile storage hierarchy, (Paragraph 0046: taught as the first and second flash memories).
- wherein accessing information in the first level consumes more energy than accessing information in the second level; and (Paragraph 0046:

taught as the high performance first flash memory and rate of power consumption thereto).

- a processor configured for writing information to the second level of storage based on energy-conserving criteria and excluding storing only minimally used portions of information (Processor as shown in Figure 1 item 20 and as taught in Paragraph 0017 and further in paragraph 0046).

As per dependent claim **22**, Rudelic teach, wherein the energy-conserving criteria comprise criteria compiled using a heuristic approach (Paragraphs 0048-0049 taught as the tracking and gathering of performance metrics).

As per dependent claim **23**, Rudelic, wherein the energy-conserving criteria comprise system state information (Paragraph 0049: taught as performance metrics).

As per dependent claim **24**, Rudelic teach, further comprising a storage input/output subsystem and wherein the system state information comprises whether the storage input/output subsystem is using one or more specific files (Paragraph 0046: taught as the determination of minimally used portions and thus files of the operating system).

As per dependent claim **25**, Rudelic teach, wherein the system state information is selected from the group consisting of: the storage input/output associated with one or more predetermined software applications; a sequence of storage input/output operations; observed interactions with the first level of the storage hierarchy and wherein the collection of heuristics infer the state of the second level of the storage hierarchy; and a type of energy source powering the system (Paragraph 0048: taught as

the migration of code due to usage corresponding to the limitation of a sequence of storage input/output operations).

As per dependent claim **26**, Rudelic teach, wherein the energy-conserving criteria comprise limiting use of parts of a file system (Paragraph 0046: taught as the migration of portions of the operating system off the first flash memory and thus limiting the use of the first flash memory).

As per dependent claim **29**, Rudelic teach, wherein the system state information comprises at least one factor from among the following factors: the storage input/output data associated with the characteristics of the connection between the first and second levels of the storage hierarchy; the storage input/output data associated with characteristics of the connection between the system and at least one second level of the storage hierarchy; the proximity of the storage input/output to events that change the state of the at least one first level of the storage hierarchy; the proximity of the storage input/output to a previous interaction with at least one first level of storage hierarchy; an indication of a hard-disk drive spin-down event; and physical characteristics of the second levels of the storage hierarchy (Paragraph 0049: taught as the performance metrics).

As per dependent claim **30**, Rudelic teach, wherein the system state information comprises physical characteristics of the second level of the non-volatile storage hierarchy (Paragraph 0049: taught as the performance metrics).

As per dependent claim **31**, Rudelic teach, wherein the second level of the non-volatile storage hierarchy is implemented using Flash memory (Paragraph 0046).

As per dependent claim **33**, Rudelic teach, wherein the processor is for removing information from the second level of non-volatile storage based on energy-conserving criteria (Paragraph 0048: taught as a code object promotion).

As per independent claim **37**, Rudelic teach,

- two levels of non-volatile storage wherein a first level is managed and a second level is unmanaged wherein storing information in managed storage consumes less system resources than storing information in unmanaged storage, the method comprising: (Paragraph 0046: taught as the first and second flash memories)
- monitoring the system to determine whether the operating state of the system satisfies one or more energy-conserving criteria; and storing only strategically selected storage data in managed storage when the operating state of the system satisfies one or more energy-conserving criteria (Paragraphs 0046-0049).

As per independent claim **38**, Rudelic teach, a computer readable medium comprising program instructions for: (Claim 12) monitoring a system to determine whether the operating state of the system satisfies one or more energy-conserving criteria; and storing only strategically selected storage data in managed non-volatile storage when the operating state of the system satisfies one or more energy-conserving criteria (Paragraphs 0046-0049).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **27-28** are rejected under 35 U.S.C. 103(a) as being obvious over Rudelic in view of Thelander et al. (U.S. 2003/0009705) hereinafter referred to as Thelander.

As per dependent claim **27**, Rudelic teach the limitations of dependent claim 3 and independent claim 1 for which dependent claim 27 depends upon.

Rudelic is silent however on, the system stores current user profiles and the system state information comprises whether storage input/output data are associated with a current user profile.

Thelander, the system stores current user profiles and the system state information comprises whether storage input/output data are associated with a current user profile (Paragraph 45 and Paragraph 48 and Paragraph 53).

Rudelic and Thelander are analogous art because they are from the same field of endeavor, namely power management in computing systems.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, having both the teachings of Rudelic and Thelander before him/her, to implement the power management profiles of Thelander into the system of Rudelic to exploit the benefit of multiple power profiles based on a user's preferences.



The motivation for doing so would have been that, the power management profile may include multiple power settings or power schemes with the same schedule, so that the user may select between different power settings or schemes to be implemented (Paragraph 45 and Paragraph 48 and Paragraph 53).

Further, it would have been obvious to implement different user profiles based on user preferences. Doing so would yield predictable results in offering the combination system the benefit of serving multiple users with different needs.

Therefore it would have been obvious to combine Rudelic with Thelander to exploit the benefit of multiple power profiles based on a user's preferences to obtain the invention as specified in claims 27 and 28.

As per dependent claim **28**, the combination of Rudelic and Thelander teach, wherein the system stores current user preferences and the system state information comprises whether storage input/output data are associated with current user preferences (Paragraph 45 and Paragraph 48 and Paragraph 53).

Claim **32** is rejected under 35 U.S.C. 103(a) as being obvious over Rudelic in view of Atkinson (U.S. 6,029,249) hereinafter referred to as Atkinson.

Rudelic teach the limitations as noted supra.

Rudelic does not teach counting remaining write cycles.

Atkinson teach, wherein the system state information comprises the number of remaining write cycles (Column 8 lines 48-51).

Rudelic and Atkinson are analogous art because they are from the same field of endeavor, namely computer system power consumption.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Rudelic and Atkinson before him/her, to implement the counter of Atkinson into Rudelic for the benefit of reducing system clock when on supplemental power to increase run time.

The motivation for doing so would have been that, a lower event count causes the frequency switching circuit to switch to a lower frequency to conserve power if the system is not already at this low frequency ... the invention allows the battery powered operating period of a computer system to be greatly extended (Column 3 lines 4-8 of Atkinson).

Therefore it would have been obvious to combine Rudelic with Atkinson for the benefit of increased run time to obtain the invention as specified in claim 32.

Claims **34-35**, **36**, and **39-40** are rejected under 35 U.S.C. 103(a) as being obvious over Rudelic in view of Kimura et al (U.S. 6,415,359) hereinafter referred to as Kimura.

As per dependent claim **34**, Rudelic teach a system that stores portions of operating systems into a hierarchical non-volatile storage device as noted above. In one embodiment, the portions are selected based on usage and stored into the different levels of flash memory based on various performance metrics that are gathered and tracked by the system of Rudelic to improve power consumption (Paragraphs 0046-0049 of Rudelic).

Rudelic however, does not teach usage of disk based non-volatile storage devices and as a result is silent on, a mapping schema between cache files in the second level of storage and disk files in the first level of storage, wherein each cache file is named with a logical cluster number of its corresponding disk file

Kimura teach usage of disk based non-volatile storage devices and the transferring of files from the disk device to a cache to improve power consumption (Abstract of Kimura) and further, a mapping schema between cache files in the second level of storage and disk files in the first level of storage, wherein each cache file is named with a logical cluster number of its corresponding disk file (Column 7 lines 31-45 of Kimura).

All of the component parts are known in both Rudelic and Kimura. The only difference is the combination of the “old elements” into a single device by combining them for usage in one system.

Thus, it would have been obvious to one of ordinary skill in the art to combine the disk device of Kimura into the system of Rudelic. This would allow the system of Rudelic to enjoy further power consumption benefits by expanding the hierarchy of non-volatile storage devices and giving an additional level of demotion to the system. Thus, objects that are given demotions based on usage from the first flash memory to the second flash memory would be continued to be monitored and further demoted to the third level offered by Kimura and accordingly would allow the system to achieve predictable results of improved power consumption.

As per dependent claim **35**, the combination of Rudelic and Kimura teach,

- comprising a hard disk drive comprising rotating magnetic media comprising the first level storage and a cache comprising the second level storage and (Column 3 line 55 to Column 4 line 15 of Kimura and the cache as taught by the flash memories of Rudelic in Paragraph 0046).
- an application-specific integrated circuit for managing the cache according to the energy-conserving criteria (Column 3 lines 41-54 of Kimura).

As per independent claim **36**, the combination of Rudelic and Kimura teach,

- first level non-volatile storage for storing information; second level non-volatile storage for storing information according to a set of energy-saving criteria; (Paragraph 0046: taught as the first and second flash memories of Rudelic)
- a battery level detector for determining the level of charge in a battery; (Column 16 lines 55-60 of Kimura).
- and a controller for storing only strategically selected storage data in the second level of storage when the battery level detector determines that the battery charge is below a pre-determined threshold of charge. (Column 4 lines 16-25 and as taught in the abstract further taught in Column 6 lines 13-30 of Kimura).

As per independent claim **39**, the combination of Rudelic and Kimura teach,

- first and second levels of non-volatile storage, wherein accessing the first level of non-volatile storage uses more energy than accessing the second

level of non-volatile storage; (Paragraph 0046: taught as the first and second flash memories of Rudelic)

- an energy use detector for determining a level of energy being used by the information handling system; and (Column 4 lines 57-67 of Kimura)
- an arbiter for storing only strategically selected storage data in the second level of the non-volatile storage when the energy use detector determines that the information handling system is being powered by a battery (Column 4 lines 16-25 and as taught in the abstract further taught in Column 6 lines 13-30 of Kimura).

As per independent claim **40**, the combination of Rudelic and Kimura teach,

- first and second levels of non-volatile storage, wherein accessing the first level of storage uses more energy than accessing the second level of storage; (Paragraph 0046: taught as the first and second flash memories of Rudelic)
- an energy use detector for determining the level of energy being used by the system; and (Column 4 lines 57-67 of Kimura)
- an arbiter for storing only strategically selected storage data in second level storage when the energy use detector determines that the system is being powered by a battery (Column 4 lines 16-25 and as taught in the abstract further taught in Column 6 lines 13-30 of Kimura).

### ***Response to Arguments***

Applicant's arguments filed 11 January 2008 have been carefully and fully considered but they are not persuasive.

With respect to applicant's argument located within the first paragraph of the second page of the remarks (numbered as page 10) which recites:

*"Therefore, Rudelic does not anticipate the invention of claim 21."*

The Examiner respectfully disagrees and wishes to note that Applicant's rationale supporting this argument appears to not be commensurate in scope with the instant claim language. Applicant's rationale (in part) recites:

*"It is possible to have a memory type A and a memory type B where accessing information in A consumes MORE energy than accessing information in B while at the same time it is true that accessing information in A requires LESS power than in B. To see how this may be true, let's denote the energy consumption in each memory type A and B as  $E_a$  and  $E_b$ , respectively. Now let's denote the power consumption in each memory type A and B as  $P_a$  and  $P_b$ , respectively, and let's denote the time it takes to access info in each memory type A and B as  $T_a$  and  $T_b$ , respectively. We can now see that if  $T_a$  is sufficiently larger than  $T_b$ , that it may be true that  $E_a = T_a * P_a > E_b = T_b * P_b$  even though  $P_a < P_b$ . Therefore, Rudelic does not anticipate the invention of claim 21."*

While Applicant's rationale and insight is appreciated, the Examiner notes the following. The instant claim broadly recites 'first and second levels of a non-volatile storage hierarchy, wherein accessing information in the first level always consumes more energy than accessing information in the second level.' Applicant has stated and supported that 'Power is defined as the rate at which work (energy) is done.' In Applicant's rationale, Applicant assumes two memory types, A and B, and that each consume P power,  $P_a$  and  $P_b$ , and that each consume E energy,  $E_a$  and  $E_b$ .

Applicant's rationale goes further to state that each memory type has a separate and distinct access time, or  $T_a$  and  $T_b$ .

The Examiner notes herein that the instant claim language does not recite and therefore does not require that the first and second levels of a non-volatile storage hierarchy have different access times.

Thus, if one instead holds  $T$  to be constant across both memory types for the access of information provided for in Applicant's rationale, the following is observed. Knowing that 'Power is defined as the rate at which work (energy) is done,' one knows then that,  $P = \frac{W}{T}$ , where  $P$  denotes Power,  $W$  denotes Work (energy), and  $T$  denotes Time. If one holds  $T$  to be constant one observes the following for the two memory types,  $P_a = \frac{W_a}{T}$  and  $P_b = \frac{W_b}{T}$ , and if one varies  $P$ , one observes that  $W$  acts directly proportionate to the change in  $P$ .

According to Rudelic paragraph 0046, "a first flash memory 170 may be different than the second flash memory 172 at least in one relative performance metric, such as the rate of power consumption." Applying this rationale to Rudelic one sees that if  $P_a$  is greater than  $P_b$  then  $W_a$  **must** be greater than  $W_b$ . Thus, since Rudelic teaches different rates of power consumption, and from the logic above, the Examiner notes that Rudelic also teaches different rates of energy consumption, anticipating that which is instantly claimed, namely, 'the first level always consumes more energy.'

With respect to applicant's argument located within the second full paragraph of the second page of the remarks (numbered as page 10) which recites:

*"Because Rudelic concerns power saving, not energy conservation, it does not teach or suggest the claimed limitations."*

The Examiner respectfully disagrees and incorporates herein the comments made *supra* showing that Rudelic teaches energy conservation through power savings. Even assuming *arguendo* that Rudelic did not teach energy conservation the Examiner notes the following. The Examiner wishes to draw Applicant's attention to Applicant's own specification paragraph 0022 which recites in part:

*'According to an embodiment of the invention the energy-conserving issues discussed above are solved by using a second level storage device (in the following, briefly referred to as cache), **that consumes less energy than the first level (main system storage) in circumstances where power savings are desired.**' (emphasis added)*

Thus, as is shown in Applicant's own specification, power savings is a desire of the instant invention. Applicant states that Rudelic concerns power savings. Accordingly, the Examiner is unsure as to how Applicant is able to perceive Rudelic as different.

With respect to applicant's argument located within the third full paragraph of the second page of the remarks (numbered as page 10) as well as the arguments located in the first two paragraphs of the last page of the instant remarks directed towards the 35 U.S.C. 103 rejections, the Examiner respectfully disagrees and refers Applicant's to the comments made *supra*.

### **Conclusion**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP



§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 21887

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KLE/mb

/Kevin L Ellis/  
Primary Examiner, Art Unit 2188